Notice of Allowability	Application No.	Applicant(s)	
	10/815,173	CHEN, INCHING	
	Examiner	Art Unit	
	Paul W. Schlie	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *an examiner initiated interviews 6/15,21,27/06 and resulting claim amendments*.

2. ☒ The allowed claim(s) is/are *1,4-13,15-26*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☐ Examiner's Statement of Reasons for Allowance
9. ☒ Other *3 corrected drawing sheets*.

EXAMINER'S AMENDMENT

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

2. Authorization for this examiner's amendment was given in a telephone interview with Mark V. Muller on 6/15,21,27/06, whereby:

Claims 1, 4-13, 15-18, and 20-24 are amended; and

Claims 2-3 and 14 are canceled; and

Drawing sheets are replaced.

3. The application has been amended as follows:

1. (Currently Amended) A method, including:

receiving an indication of a plurality of memory addresses, a protocol type, and an operation type;

selecting a memory bank group consisting of one or more of a plurality of memory banks, wherein said group is responsive to one of said plurality of memory addresses and the operation type if said protocol type comprises a single-instruction multiple-data (SIMD) protocol type;

selecting a plurality of memory bank groups each consisting of one or more of said plurality of memory banks, where each of said plurality of groups is correspondingly uniquely responsive to one of said plurality of memory addresses and the operation type if said protocol type comprises a multiple-instruction multiple-data (MIMD) protocol type; and

receiving or alternately returning an indication of data corresponding to said memory bank group selection and corresponding operation type indication.

~~selecting a memory access group size of about 2^N memory banks responsive to receiving an indication of a change in a protocol type, wherein the group is selected from a number B of banks, wherein N is associated with the protocol type, and wherein N is selected so that 2^N is less than or equal to B so that a plurality of logical addresses associated with the 2^N memory banks is mapped to a plurality of physical addresses associated with the number B of banks.~~

2. (Canceled)

3. (Canceled)

4. (Currently Amended) The method of claim 1, further including:
responsive to receiving the indication of the protocol type, selecting a first memory access group size for a first data processing unit different than a second memory access group size selected for a second data processing unit~~, wherein the first data processing unit and the second data processing unit are capable of addressing the number B of banks~~.

5. (Currently Amended) The method of claim 1, wherein the indication of the [[a]] protocol type is selected from one of a hardware indication and a software indication.

6. (Currently Amended) The method of claim 4[[1]], wherein the first memory access group size is associated with a selected number of access bits.

7. (Currently Amended) The method of claim 4[[1]], further including:
configuring a crossbar to operate using the first memory access group size responsive to receiving the indication of the ~~change in the~~ protocol type.

8. (Currently Amended) An article including a machine-accessible storage medium ~~having associated information~~ comprising a computer executable program~~, wherein the information,~~ which when executed ~~when accessed,~~ results in a machine performing:

receiving an indication of a plurality of memory addresses, a protocol type, and an operation type;

selecting a memory bank group consisting of one or more of a plurality of memory banks, wherein said group is responsive to one of said plurality of memory addresses and the operation type if said protocol type comprises a single-instruction multiple-data (SIMD) protocol type;

selecting a plurality of memory bank groups each consisting of one or more of said plurality of memory banks, wherein each of said plurality of groups is correspondingly uniquely responsive to one of said plurality of memory addresses and the operation type if said protocol type comprises a multiple-instruction multiple-data (MIMD) protocol type; and

receiving or alternately returning an indication of data corresponding to said memory bank group selection and corresponding operation type indication.

~~selecting a memory access group size of about 2^N memory banks responsive to receiving an indication of a change in a protocol type, wherein the group is selected from a number B of banks, wherein N is associated with the protocol type, and wherein N is selected so that 2^N is less than or equal to B so that a plurality of logical addresses associated with the 2^N memory banks is mapped to a plurality of physical addresses associated with the number B of banks.~~

9. (Currently Amended) The article of claim 8, wherein the protocol type is selected from at least one of a SIMD ~~single-instruction multiple-data operation~~ protocol type, a MIMD ~~multiple-instruction multiple-data operation~~ protocol type, and a combination of the SIMD ~~single-instruction multiple-data operation~~ protocol type and the MIMD ~~multiple-instruction multiple-data operation~~ protocol type.

10. (Currently Amended) The article of claim 8, wherein the information, when accessed, results in a machine performing:

responsive to receiving the indication of the protocol type, selecting a first memory access group size for a first data processing unit different than a second memory access group size; and

selecting the second memory access group size for a second data processing unit~~, wherein the first data processing unit and the second data processing unit are capable of addressing the number B of banks~~.

11. (Currently Amended) An apparatus, including:

an address interface to couple to at least one data processing unit, the address interface to receive an indication of a plurality of memory addresses, a protocol type, and an operation type; to select a memory bank group consisting of one or more of a plurality of memory banks, wherein said group is responsive to one of said plurality of memory addresses and the operation type if said protocol type comprises a single-instruction multiple-data (SIMD) protocol type; to select a plurality of memory bank groups each consisting of one or more of said plurality of memory banks, wherein each of said plurality of groups is correspondingly uniquely responsive to one of said plurality of memory addresses and the operation type if said protocol type comprises a multiple-instruction multiple-data (MIMD) protocol type; and to receive or alternately return an indication of data corresponding to said memory bank group selection and corresponding operation type indication.

~~a selection module to select a memory access group size for at least one data processing unit of about 2^N memory banks responsive to receiving an indication of a change in a protocol type, wherein the group is selected from a number B of banks, wherein N is associated with the protocol type, and wherein N is selected so that 2^N is less than or equal to B so that a plurality of logical addresses associated with the 2^N memory banks is mapped to a plurality of physical addresses associated with the number B of banks.~~

12. (Currently Amended) The apparatus of claim 11, further including:

a plurality of data processing units including the at least one data processing units~~, wherein the plurality of data processing units is capable of addressing the number B of banks~~.

13. (Currently Amended) The apparatus of claim 12, wherein the plurality of data processing units ~~and the number B of banks~~ are included in a single processing element.

14. (Canceled)

15. (Currently Amended) The apparatus of claim 12, further including:

a hardware address generator to generate the plurality of memory addresses~~an address located in the 2^N memory banks~~.

16. (Currently Amended) A system, including:

an address interface to couple to at least one data processing unit, the address interface to receive an indication of a plurality of memory addresses, a protocol type, and an operation type; to select a memory bank group consisting of one or more of a plurality of memory banks, wherein said group is responsive to one of said plurality of memory addresses and the operation type if said protocol type comprises a single-instruction multiple-data (SIMD) protocol type; to select a plurality of memory bank groups each consisting of one or more of said plurality of memory banks, wherein each of said plurality of groups is correspondingly uniquely responsive to one of said plurality of memory addresses and the operation type if said protocol type comprises a multiple-instruction multiple-data (MIMD) protocol type; and to receive or alternately return an indication of data corresponding to said memory bank group selection and corresponding operation type indication;

~~a selection module to select a memory access group size of about 2^N memory banks responsive to receiving an indication of a change in a protocol type, wherein~~

~~the group is selected from a number B of banks, wherein N is associated with the protocol type, and wherein N is selected so that 2^N is less than or equal to B so that a plurality of logical addresses associated with the 2^N memory banks is mapped to a plurality of physical addresses associated with a the number B of banks;~~

a data processing unit capable of addressing the memory bank group selection~~number B of banks~~; and

an omnidirectional antenna to transmit data processed by the data processing unit.

17. (Currently Amended) The system of claim 16, further including:

a bus to couple the data processing unit to the memory bank group selection~~one of the number B of banks~~.

18. (Currently Amended) The system of claim 16, further including:

a memory to couple to the data processing unit and to store a plurality of memory access group sizes indexed to a corresponding plurality of protocol types.

19. (Original) The system of claim 16, further including:

a transceiver to couple a processing element including the data processing unit to the omnidirectional antenna.

20. (Currently Amended) An apparatus, including:

a plurality ~~number B~~ of memory banks addressable using an address interface to couple to at least one data processing unit, the address interface to receive an indication of a plurality of memory addresses, a protocol type, and an operation type; to select a memory bank group consisting of one or more of the plurality of memory banks, wherein said group is responsive to one of said plurality of memory addresses and the operation type if said protocol type comprises a single-instruction multiple-data (SIMD) protocol type; to select a plurality of memory bank groups each consisting of one or more of said plurality of memory banks, wherein each of said

plurality of groups is correspondingly uniquely responsive to one of said plurality of memory addresses and the operation type if said protocol type comprises a multiple-instruction multiple-data (MIMD) protocol type; and to receive or alternately return an indication of data corresponding to said memory bank group selection and corresponding operation type indication.

~~a memory access group size of about 2^N memory banks responsive to receiving an indication of a change in a protocol type, wherein the group is selected from the number B of banks, wherein N is associated with the protocol type and selected so that 2^N is less than or equal to B and wherein the protocol type consists of a single-instruction multiple-data operation type, a multiple-instruction multiple-data operation type, and a combination of the single-instruction multiple-data operation type and the multiple-instruction multiple-data operation type.~~

21. (Currently Amended) The apparatus of claim 20, wherein the plurality of memory banks has a memory access group size, and wherein the memory access group size is reprogrammable and is selectable in software.

22. (Currently Amended) The apparatus of claim 20, further including:

a hardware element to store a plurality of output indications based on a corresponding plurality of memory access group sizes and responsive to a corresponding plurality of protocol type indications including the indication of the protocol type.

23. (Currently Amended) A method, including:

controlling a bandwidth of a memory coupled to a plurality of data processing units responsive to an address interface receiving an indication of a plurality of memory addresses, a protocol type, and an operation type; selecting a memory bank group consisting of one or more of a plurality of memory banks, wherein said group is responsive to one of said plurality of memory addresses and the operation type if said protocol type comprises a single-instruction multiple-data (SIMD)

protocol type; and selecting a plurality of memory bank groups each consisting of one or more of said plurality of memory banks, wherein each of said plurality of groups is correspondingly uniquely responsive to one of said plurality of memory addresses and the operation type if said protocol type comprises a multiple-instruction multiple-data (MIMD) protocol type; and receiving or alternately returning an indication of data corresponding to said memory bank group selection and corresponding operation type indication~~a number of data processing units in use so that a plurality of logical addresses associated with the memory is mapped to a plurality of physical addresses associated with the memory~~.

24. (Currently Amended) The method of claim 23, wherein a [[the]] number of data processing units in use selected from the plurality of data processing units is responsive to the [[an]] indication of the protocol type provided by an application to be executed.

25. (Original) The method of claim 23, wherein the bandwidth of the memory is associated with a selected number of access bits provided by the plurality of data processing units.

26. (Original) The method of claim 23, wherein controlling the bandwidth further includes:

controlling an address mapping function of the memory.

Figure 2 amended, as per separately attached "Replacement Drawing Sheets".

Conclusion

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul W. Schlie whose telephone number is 571-272-6765. The examiner can normally be reached on Mon-Thu 8:00-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Kim can be reached on 517-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

PIERRE BATAILLE
PRIMARY EXAMINER
6/28/06

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MODE OF ACCESSES	BANK 0	BANK 1	BANK 2	BANK 3
32-BIT ACCESS:	0 → 0	0 → 1	0 → 2	0 → 3
	1 → 4	1 → 5	1 → 6	1 → 7
	2 → 8	2 → 9	2 → 10	2 → 11
	3 → 12	3 → 13	3 → 14	3 → 15
64-BIT ACCESS:	0 → 0	1 → 1	0 → 2	1 → 3
	2 → 4	3 → 5	2 → 6	3 → 7
	4 → 8	5 → 9	4 → 10	5 → 11
	6 → 12	7 → 13	6 → 14	7 → 15
128-BIT ACCESS:	0 → 0	1 → 1	2 → 2	3 → 3
	4 → 4	5 → 5	6 → 6	7 → 7
	8 → 8	9 → 9	10 → 10	11 → 11
	12 → 12	13 → 13	14 → 14	15 → 15

FIG. 1

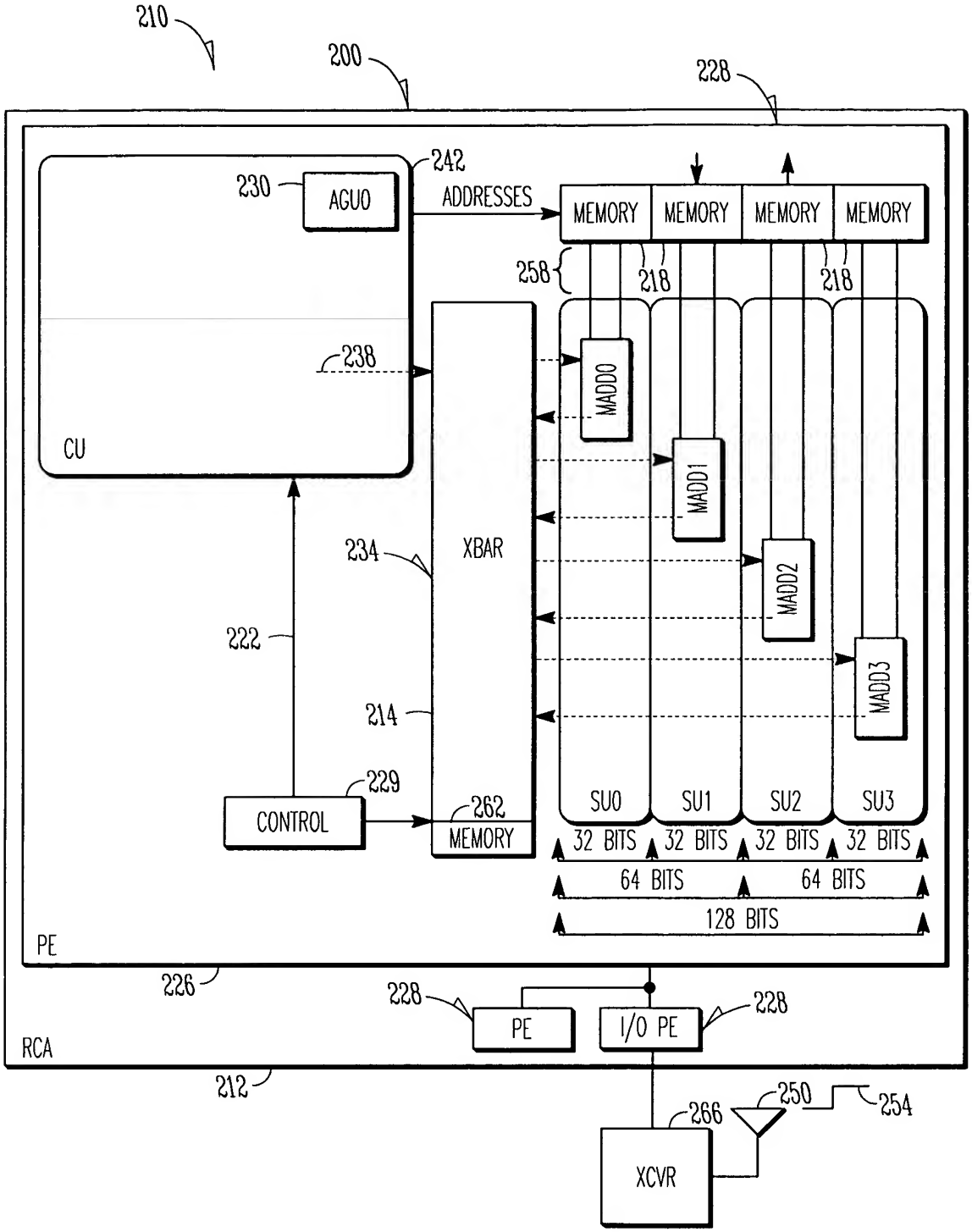
210
200
228
242
230
AGU0
ADDRESSES
MEMORY
MEMORY
MEMORY
MEMORY
258
218
218
238
MADD0
MADD1
MADD2
MADD3
CU
XBAR
234
222
214
229
CONTROL
262
MEMORY
SU0
SU1
SU2
SU3
32 BITS
32 BITS
32 BITS
32 BITS
64 BITS
64 BITS
128 BITS
PE
226
228
PE
I/O PE
228
RCA
212
250
254
266
XCVR

FIG. 2

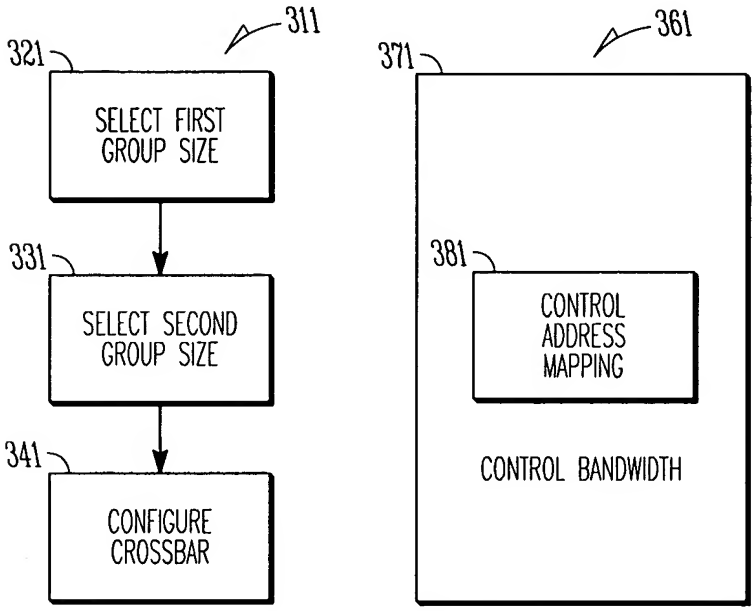
311
321
SELECT FIRST GROUP SIZE
331
SELECT SECOND GROUP SIZE
341
CONFIGURE CROSSBAR
361
371
381
CONTROL ADDRESS MAPPING
CONTROL BANDWIDTH

FIG. 3

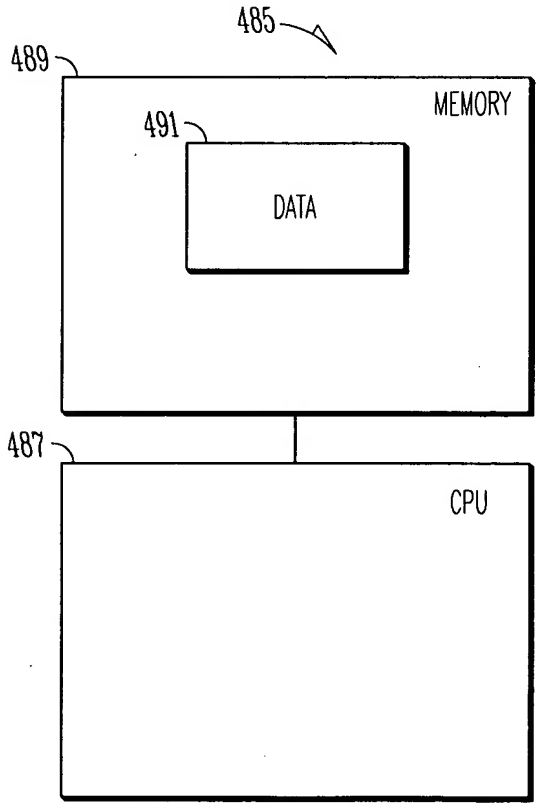
485
489
MEMORY
491
DATA
487
CPU

FIG. 4